ABSTRACT OF THE DISCLOSURE

A systematic method for single-rail domino logic circuits is provided, in which inverting and non-monotonic logic functions can be integrated into a pipelined system with almost zero overhead. This logic family, called Clock Logic (CL)-domino is functionally complete while tolerating skew and minimizing the number of clock phases that must be distributed. Simulation results for a CL-domino ALU at 1-GHz under high skew (1-FO4) conditions, shows a power reduction of 41% over the same ALU implemented in dual-rail skew-tolerant domino logic. This power reduction incurs no performance penalty over dual-rail techniques, although in some cases additional design effort is required.